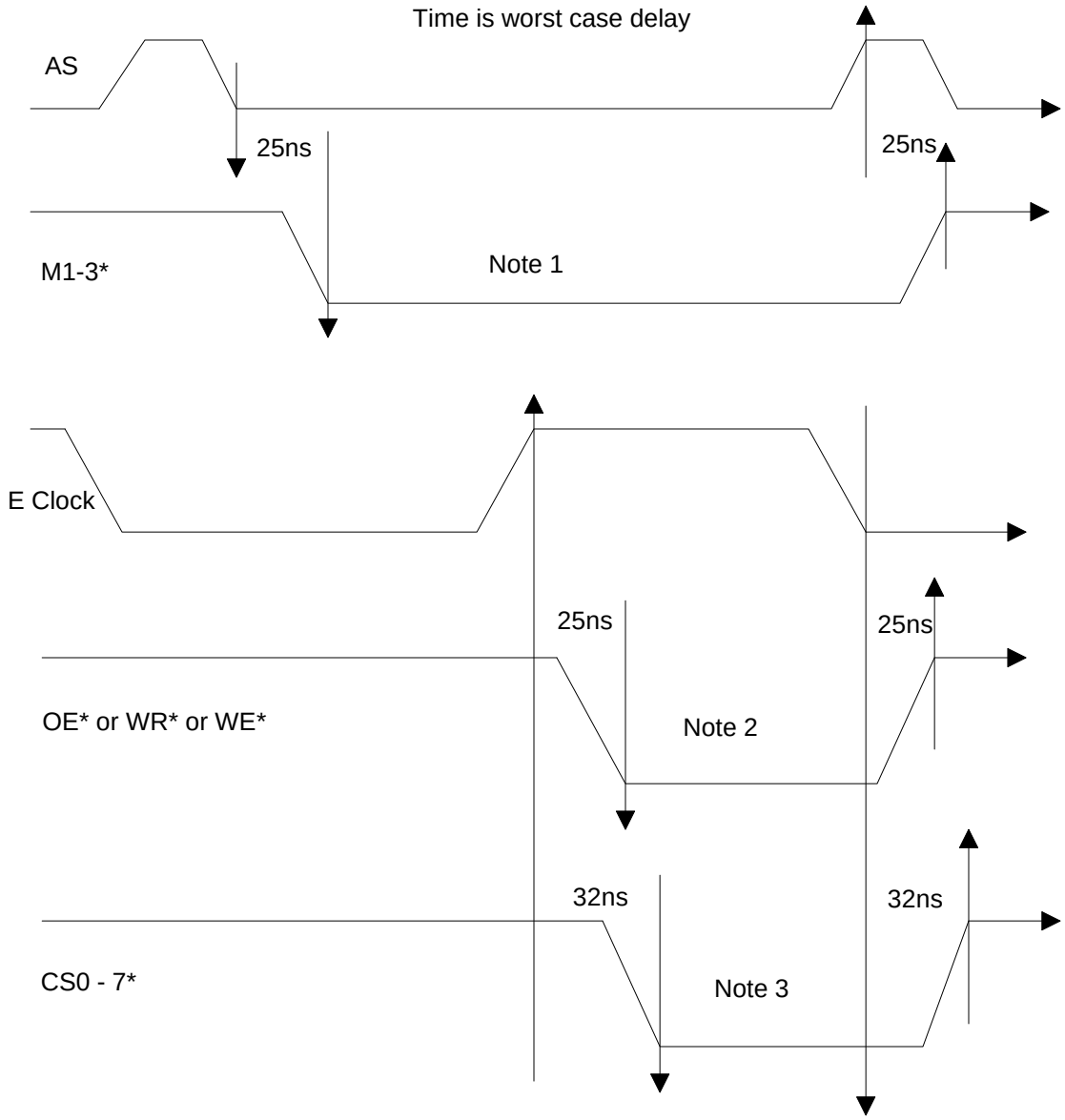
68HC11 Board Timing



Note 1: M1-3 chip select delay is determined by 16V8 PLD rating and maybe 15ns.
Note 2: OE, WR, and WE delay is determined by 16V8 PLD rating and maybe 15ns.
Note 3: CS0 - 7 delay is determined by 16V8 PLD delay plus 74HC138 decoder delay and maybe 22ns total delay. EVBU board has Sync jumper which when installed will reduce cycle end delay to 8ns typical.