CMM-11A8

68HC11

SINGLE BOARD COMPUTER

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1. GETTING STARTED

The Axiom CMM11 single board computer is a fully functional miniature development board complete with EEprom program memory, regulated power supply, LCD Interface, Keypad Interface, and buss expansion. The CMM11 is preprogrammed with the buffalo monitor at the factory. Primary interface to the board is through the COM1 serial port. Connect COM1 serial port to a serial port on the PC using a standard male to female 9 pin serial cable.

Communications settings are 9600 baud, 1start, 1stop, 8data, no parity. Most any communications program that can be set to these parameters will work with this system. Even the Terminal feature in Windows 3.1* will do an adequate job.

After the serial cable is connected, apply 6V to 15VDC power to the board at the battery connection. Use caution and observe the polarity of the power connections. If everything is working properly, the Buffalo Monitor prompt will appear on the PC display.

2. PROGRAMMING EEPROM MEMORY

Programming is performed by using the CMM11.EXE program supplied on the utility disk. The CMM11 programming utility allows external EEprom Program Memory, Configuration register, and internal 68HC11 EEprom programming. CMM11.EXE is menu driven with an on-line help.

CMM11.EXE interfaces to the CMM11 board while the 68HC11 is in Bootstrap Mode. For CMM11 programming follow the steps below:

1. Install Jumpers JP1, JP2, and JP6.
2. A RESET jumper can be installed on BUS_PORT Connector pins 43 and 44.
3. Apply power to CMM11 board and start CMM11.EXE program. Select PC COM Port in use and operation from main menu.
4. Verify that External Program Memory S19 object files are properly addressed.
5. After programming, remove JP1, JP2, and JP6 for normal operation.

3. SERIAL PORT COM1

COM1 is a simple, three wire asynchronous serial interface with hard wired Clear to Send (CTS) and Data Terminal Ready (DTR). It is driven by the 68HC11 internal SCI port using I/O pins PD0 and PD1. These two logic level signals are coupled thru a RS232 level shifter to the COM1 connector. The interface can be snapped off to reduce board size if not required after programming.

SERIAL PORT CONNECTIONS

COM1
DB9S Style Connector

Permanent Jumpers between following pins:

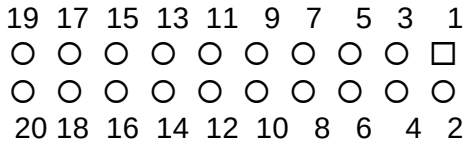
○ 1 4 to 1 and 6, 7 to 8

4. PARALLEL PORTS

The 68HC11 is configured for expanded/multiplexed mode. It uses Port B and Port C for address and data buss to external memory and memory mapped I/O devices. This leaves CPU Port D, Port A, and Port E to provide all other parallel I/O from the controller. All remaining CPU port lines serve dual functions with internal CPU peripherals such as the timer subsystem and port A, the A/D converter on port E, and the SPI or SCI on port D. All port lines are limited to sinking and sourcing approximately 1mA. maximum.

CPU_PORT CONNECTOR

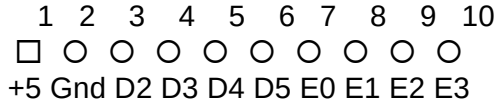
The CPU_PORT connector is a dual row 10 pin Berg-style connector (20 pins total) which is configured as follows:



PIN	FUNCTION	PIN	FUNCTION
1	PA0	2	PA1
3	PA2	4	PA3
5	PA4	6	PA5
7	PA6	8	PA7
9	PE7	10	PE3
11	PE6	12	PE2
13	PE5	14	PE1
15	PE4	16	PE0
17	VRL	18	VRH
19	GND	20	+5V

SS:KEYPAD CONNECTOR

The SS:Keypad Connector is an ten position connector that implements 4 bits of PortD and 4 bits of PortE as a simple serial or keypad interface. This interface provides connection for the SPI port on PortD as a Simple Serial interface or may be implemented as a software keyscan for a passive Keypad. Keypad Connector pinout follows:



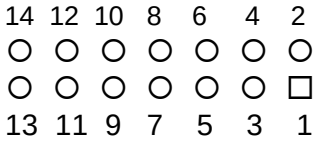
PD0 and PD1 are used by the HC11 SCI to implement COM1. PD<2:5> are used by the HC11 SPI to implement the SS:KEYPAD port. These port D lines can also be used for parallel I/O, but then they will not be available for COM1 and the SS:KEYPAD port. Use caution when assigning port D lines to functions other than COM1 and the SS:KEYPAD port .

PE0 to PE3 are used on the SS:KEYPAD port as row inputs. Use caution if used as A/D channel inputs as the SS:KEYPAD port has 100K pull-down resistors attached to these lines. R8, R9, R10, and R21 can be removed to isolate PortE 0 to 3 for A/D functions.

5. LCD INTERFACE

The LCD interface is connected to the data buss and memory mapped to locations B5F0 and B5F1. It supports all OPTREX* DMC series displays up to 80 characters. Power, ground, and VEE are available at the LCD_PORT connector on the card. The LCD VEE (Contrast) pin is normally grounded on the CMM11 board. VEE (Contrast) Adjustment can be supplied by factory option.

LCD_PORT CONNECTOR



PIN	FUNCTION	PIN	FUNCTION
1	GND	2	+5
3	VEE	4	A0
5	R/W	6	LCDCS
7	D0	8	D1
9	D2	10	D3
11	D4	12	D5
13	D6	14	D7

* OPTREX is a registered trademark of OPTREX, INC.

6. ADDRESS DECODING AND MEMORY MAP

Address decoding is accomplished using a GAL16V8 programmable logic device. Address lines A<8:15>, AS (address strobe), R/W (read/write), and E (clock) are processed to provide the memory control signals as shown below by default. Custom configurations, differing from that shown below, are also possible. Contact the factory for assistance in redefining the memory map if required.

OE - Output enable to U5, U6, and BUS_PORT

WR- Write enable to U5 and BUS_PORT. JP6 enables WR to U6.

M1- Chip select to U5 RAM. CMM11A8-8 = 8K from $2000 to $3FFF (mirrored at $6000 to $7FFF), CMM11A8-32 = 32K from $0000 to $7FFF.

M2- Chip select to BUS_PORT. CMM11A8-8 = 24K from $8000 and $DFFF, except $B580 through $B7FF inclusive. Not Available on CMM11A8-32.

M3- Chip select to U6. CMM11A8-8 = 8K from $E000 to $FFFF. CMM11A8-32 = 32K from $8000 to $FFFF except $B580 through $B7FF.

P- Peripheral Access CS0 - CS7. B580 through B5FF.

All of these signals except P are active low. P is active high. Signal line M2 is dedicated to the BUS_PORT expansion connector allowing M2 to work in conjunction with the CS and Address lines to implement off board, page banked memory on the CMM11A8-8 board.

U5 is intended to be either an 8k or a 32k RAM. U7 is to be used primarily for Program EEPROM but it can also accomodate EPROM for lower board cost at high volumes. Contact Axiom with your requirement for custom configurations. Peripheral Access 'P' is used in conjunction with A<4:6>, and AS to generate CS<0:7>. Each of these eight chip selects controls sixteen bytes in the memory map from B580 through B5FF. CS7 is used by the LCD_PORT. CS<7:0> are brought out to the BUS_PORT where they can be used to control peripherals external to the CMM11 board. See the Memory Map for further clarification.

MEMORY DEVICE OPTION SELECTION JUMPERS

Device selection jumpers for U5 and U6 are surface mount component pads on the bottom of the board. These jumpers are installed at the factory in the default positions but are described here for convience. The U2 16V8 GAL is programmed for the specific memory size at the factory, jumper options may have no effect on actual memory map of memory device.

CMM11A8-8 Defaults:

U5 - **JP3** for **8K** device = **Closed:** 8K from 2000 hex to 3FFF hex and mirrored at 6000 - 7FFF.
Recommended position for Buffalo

Monitor and Small C operation.
No segmentation occurs.

Option: **Open:** 8K from 0000 hex to 1FFF hex and mirrored at 2000 - 3FFF, 4000 - 5FFF, and 6000 - 7FFF. This position will allow CPU internal Ram and I/O ports to segment the 8K address space.

U6 - JP4 Closed, JP5 Open = 8K from E000 hex to FFFF hex.
JP6 = Write Protect if Open or Write Enable if Closed.

CMM11A8-32 Defaults:

U5 - **JP3** for **32K** device = **Closed:** 32K from 0000 hex to 7FFF hex

U6 - JP4 Closed, JP5 Open = 32K from 8000 hex to FFFF hex. Excluding B580 through B7FF hex.
JP6 = Write Protect if Open or Write Enable if Closed.

MEMORY MAP

This memory map is for an HC11A8 as used in this development board. Other HC11 devices in the A series may also be used, as well as devices in the E and F series. These optional devices differ in the amount of internal RAM, ROM, EEPROM available and the factory default value of the CONFIG register. Consult the technical reference for the specific device you are using for additional information.

	CMD11A8-8	**CMD11A8-32**
$FFFF	EEPROM (U6) PROGRAM 8 K	EEPROM (U6) PROGRAM 18.4K
$E000		
$DFFF	M2 Select (BUS_PORT) 10.2K	
$B800		
$B7FF	HC11 INTERNAL EEPROM 512 Byte	
$B600		
$B5FF	CS7 (BUS_PORT) 12Byte	
$B5F4		
$B5F3	$B5F2 - $B5F3 = Reserved $B5F1 = Data Register LCD_PORT $B5F0 = Command Register 4 Byte	
$B5F0		
$B5EF	CS6 (BUS_PORT) 16 Byte	
$B5E0		
$B5DF	CS5 (BUS_PORT) 16 Byte	
$B5D0		
$B5CF	CS4 (BUS_PORT) 16 Byte	
$B5C0		
$B5BF	CS3 (BUS_PORT) 16 Byte	

$B5B0				
$B5AF	CS2 (BUS_PORT)			16 Byte
$B5A0				
$B59F	CS1 (BUS_PORT)			16 Byte
$B590				
$B58F	CS0 (BUS_PORT)			16 Byte
$B580				
$B57F	M2 Select (BUS_PORT)	13.7K	EEPROM (U6) PROGRAM	13.7K
$8000				
$7FFF	RAM (U5) {mirrored}	8K		
$6000				
$3FFF	RAM (U5) {mirrored}	8K	RAM (U5)	28.6K
$2000				

MEMORY MAP CONTINUED:

$1040			
$103F	CONFIG		
$103D	INIT		
$103C	HPRIO		
$1039	OPTION		
$102F	SCDR		
$102E	SCSR2	HC11 INTERNAL REGISTERS	
$102D	SCCR2	PARTIAL LISTING	
$102C	SCCR1	SEE HC11 REFERENCE MANUAL	
$102B	BAUD	FOR COMPLETE LISTING AND	
$1029	SPSR	USAGE INFORMATION	
$1028	SPCR		
$1026	PACTL	THIS REGISTER BLOCK CAN BE	
$1025	TFLG2	RELOCATED TO ANY UNUSED	
$1024	TMSK2	4K BOUNDARY TO PROVIDE A	
$1020	TCTL1	CONTIGUOUS RAM SPACE	
$100F	TCNT		
$100E	TCNT	THE REGISTERS WILL APPEAR AS	
$100D	OC1D	SHOWN HERE ON INITIAL POWER	
$100C	OC1M	UP/RESET OF THE CMM11A8 BOARD	
$100B	CFORC		
$100A	PORTE		
$1009	DDRD		
$1008	PORTD		
$1007	DDRC		
$1005	PORTCL		
$1004	PORTB		
$1003	PORTC		64 Byte
$1002	PIOC		
$1000	PORTA		
$0FFF			
	Not Used	RAM (U5)	3.8 K
$00FF			
	HC11 INTERNAL RAM		256 Byte
$0000			

7. RESET

Reset is provided by an 8054 low voltage detector when Vdd falls below approximately 4.4 volts. If the CMM11 board is operated from batteries, the standard battery source should be 6V (4 x 1.5V AA cells) for optimum life. Allowing the MCU to sleep for maximum battery life will require an external wakeup source connected to the IRQ pad and software support.

8. MODE SELECT

The MODA and MODB pins of the HC11 are pulled high by two 10k resistors. This is the normal EXPANDED MODE configuration. Installing option jumpers JP1 and JP2 and applying a RESET will place the MCU in BOOTSTRAP MODE. This mode is required for programming the CMM11 board with CMM11.EXE software.

These two jumpers allow selection of any of the following modes of operation:

JP1	JP2	
MODA	**MODB**	**MODE OF OPERATION**
closed	closed	Special Bootstrap
closed	open	Special Test
open	closed	Normal Single Chip
open	open	Normal Expanded (default)

9. A/D REFERENCE

The VRH and VRL lines from the HC11 are connected to +5v through R3 and to ground through R2 respectively. These two surface mount resistors are on the bottom (solder) side of the circuit board. The resistors are indentified on the silk screen by their reference designators and the dashed line box that surrounds them. The appropriate resistor(s) need to be removed in order to apply an external reference to the VRH and/or VRL connections on the MCU_PORT.

10. EXPANSION BUS

The BUS_PORT supports off-board devices. Power (+5V), ground, address lines, data lines, and control lines are brought out to this 40 pin connector. Pin

assignments are shown on page 2 of the schematic and are listed below for convenience.

BUS_PORT			PIN	FUNCTION	PIN	FUNCTION
1	□ ○	2	1	GND	2	D3
3	○ ○	4	3	D2	4	D4
5	○ ○	6	5	D1	6	D5
7	○ ○	8	7	D0	8	D6
9	○ ○	10	9	A0	10	D7
11	○ ○	12	11	A1	12	A2
13	○ ○	14	13	A10	14	A3
15	○ ○	16	15	OE	16	A4
17	○ ○	18	17	A11	18	A5
19	○ ○	20	19	A9	20	A6
21	○ ○	22	21	A8	22	A7
23	○ ○	24	23	A12	24	A13
25	○ ○	26	25	W/R	26	CS0
27	○ ○	28	27	CS1	28	CS2
29	○ ○	30	29	CS3	30	CS4
31	○ ○	32	31	CS5	32	IRQ
33	○ ○	34	33	+5	34	M2
35	○ ○	36	35	R/W	36	CS6
37	○ ○	38	37	E	38	CS7
39	○ ○	40	39	GND	40	RESET

11. TROUBLESHOOTING

The board is fully tested and operational before shipping. If it fails to function properly, inspect the board for obvious physical damage first. Ensure that JP1 and JP2 are NOT installed unless programming is being performed. Verify the communications setup as described under GETTING STARTED.

If the problem is bad checksum during programming, make sure your code is addressed to the correct memory space. The programmer will attempt to write

wherever the S19 record indicates. Verify JP6 is Installed or the external EEprom will not program.

The most common problems are improperly configured communications parameters, and attempting to use the wrong COM port on the PC. Verify that your communications port is working by substituting a known good serial device, or by doing a loop back diagnostic.

Verify the power source. Input voltage should not be below 6 volts DC.

APPENDIX A. SCHEMATIC and MECHANICAL

APPENDIX B. STANDARD LCD AND KEYPAD DATA SHEETS